Amendments to the Abstract:

~~ABSTARCT~~ ABSTRACT OF THE DISCLOSURE

~~There are provided a~~ A semiconductor memory device ~~incorporating~~ incorporates an ECC circuit which enables an efficient test of the device with high accuracy ~~by~~ using a simplified structure, and which can shorten the test time ~~and a test method thereof. A semiconductor memory device has an~~. The ECC circuit is capable of correcting, from an m–bit information code and an n–bit check code that have been stored in an information storing part, an error of the information code to x bits, and a parallel test circuit is provided for receiving an information code and a check code for the test with the same bits stored in the information storing part and ~~deciding~~ for determining that a product having a defect with ~~the~~ x+1 bits or more ~~as being~~ is defective. The parallel test circuit ~~decides~~ determines that a chip having a defect with ~~the~~ x+1 bits or more for one piece of position information ~~as a~~ is defective chip.